Complementary HBT Push–Pull Amplifier by Selective MBE

K. W. Kobayashi, D. K. Umemoto, J. R. Velebir, A. K. Oki, and D. C. Streit

Abstract— **Microwave performance results are presented of the first monolithically integrated GaAs-AlGaAs complementary HBT push–pull amplifier fabricated using selective molecular beam epitaxy and a merged HBT process. The push–pull amplifier integrates four n-p-n transistors with one p-n-p transistor on the same GaAs chip. The amplifier has a sharp dc characteristic curve with no cross-over offset, a voltage swing of 6.3 V using a 9 V supply, and a linear voltage gain of 20. The bandwidth is dc to 2.5 GHz, with a saturated output power of 7.4 dBm at 2.5 GHz.**

INTEGRATED complementary n-p-n/p-n-p transistors add new dimensions to the application base of heterojunction bipolar transistor (HBT) technology. Power consumption can be reduced and circuit performance and efficiency can be improved using complemetary HBT's. One such example is the use of active loads, which can replace load resistors of differential pair stages in operatonal amplifiers. This would reduce the voltage supply required, and increase the voltage gain of the differential stage.

Another application of complementary HBT's is for high efficiency push–pull power amplifiers. These can be realized without the need for complex transformer circuits to implement 180 degree baluns. The push–pull amplifier is a basic building block for many bipolar applications, including output stages in operational amplifiers, oscillators, and power amplifiers which need to efficiently drive low impedance loads. The dc characteristics of complementary HBT's using selective MOVPE has been reported [1]. We present here the dc and microwave results of a monolithically integrated complementary HBT push–pull amplifier fabricated using selective MBE.

The fabrication of n-p-n and p-n-p HBT devices on the same GaAs substrate using selective MBE and a merged HBT processing technology were previously described [2], [3]. The current process focuses on the complete integration of p-n-p/n-p-n HBT circuits, with special consideration given to the interconnection of the complementary transistors. The HBT profiles used here are shown in Fig. 1. The p-n-p profile was grown first by MBE on a 3-inch undoped (100) GaAs substrate in a conventional manner. The silicon doping in the 80-nm base was exponentially graded from $1 \times 10^{18}\,\mathrm{cm}^{-3}$ at the collector edge to $7 \times 10^{18}\,\mathrm{cm}^{-3}$ at the emitter edge. Graded doping has been shown to improve the performance of both p-n-p [4], [5] and n-p-n [6] HBT's. Properly optimized, p-n-p devices have potential performance near that of n-p-n devices [7].

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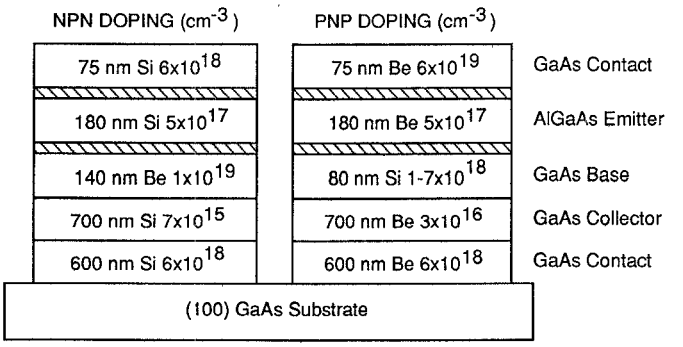

Fig. 1. Device profiles for n-p-n and p-n-p HBT's grown by selective MBE.

The wafer was removed from the MBE system following the p-n-p layer deposition and patterned with silicon nitride. The n-p-n profile was then deposited. The n-p-n layers deposited on the silicon nitride were polycrystalline, while the layers deposited on the GaAs substrate between the p-n-p islands were high quality single crystal. The polycrystalline n-p-n layers and the silicon nitride mask were removed with selective etches. The n-p-n and p-n-p devices were fabricated using a merged HBT process [2]. This technique allows both the n-p-n and p-n-p transistors to be processed simultaneously. Single etches were used to access the base and collector contacts for both types of devices, and single evaporations were used for the n-type and p-type ohmic contacts. Device isolation within the individual n-type and p-type islands was achieved with multiple boron implants.

The implementation of the monolithic complementary process is shown in Fig. 2. This scanning electron micrograph shows the p-n-p and n-p-n islands, which are physically isolated from each other during the selective MBE deposition sequence. The first interconnect and top metal evaporations total $\sim 2\ \mu$m Au, and are used to connect the p-n-p and n-p-n devices on the seperate material islands. This interconnect topology is not significantly different from that of a noncomplementary technology, although the mesa height is $\sim 0.6\ \mu$m greater.

The n-p-n device has a common emitter current gain $\beta = 17$ at $I_c = 4$ mA, with an Early voltage of ~ 400 V. V_{ce}(sat) is between 0.7 and 1.25 V, and is a function of collector current. The p-n-p device has $\beta = 117$ at $I_c = 2.3$ mA, with an early voltage of 105 V. V_{ce}(sat) ranges from -0.8 to -2.0 volts. The p-n-p device has a wider Vce(sat) range than the n-p-n as a result of higher collector resistance. The MBE growth was optimized for the p-n-p transistor

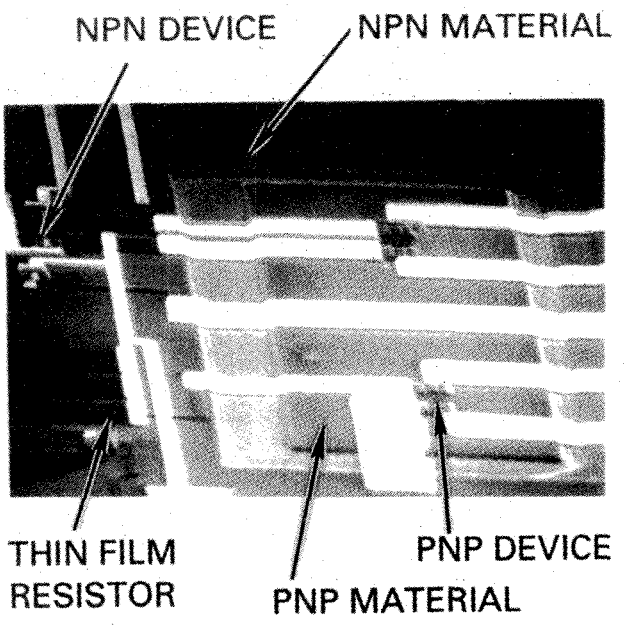

Fig. 2. Scanning electron micrograph of processed complementary HBT push–pull amplifier, showing distinct p-n-p and n-p-n material and devices with interconnect topology.

performance using exponentially graded base doping. As a result, consistently high β was measured across the wafer. P-n-p HBT devices normally have low β that imposes an inherent limitation on complementary circuits. Cutoff frequencies of 12.5 and 22 GHz were measured for the $3 \times 10\ \mu m^2$ p-n-p and n-p-n devices, respectively, at a current density of $1.3 \times 10^4\ A/cm^2$.

The complementary HBT push–pull amplifier schematic is shown in Fig. 3, together with the amplifier Vout vs. Vin voltage characteristics. This amplifier design is a basic bipolar circuit building block and contains one 750-Ω thin-film resistor for biasing, 2 n-p-n transistors, 2 n-p-n diode connected transistors, and one p-n-p transistor. The output transistors $Q2$ and $Q3$ are quad $3 \times 10\ \mu m^2$ emitter devices. The two diode connected n-p-n transistors serve to reduce the offset voltage between the turn-on/turn-off thresholds of the n-p-n/p-n-p transistors. The circuit layout was designed for easy on-wafer characterization. The V_{out} vs. V_{in} curve shows a sharp monotonic voltage transition, characteristic of high linear gain and well-defined saturation levels. The measured voltage gain is 20, while the voltage swing is 6.3 V peak-to-peak using a 9 V supply, with 20 μA of leakage current at the output. The amplifier dc-functional yield across the wafer was $\sim 70\%$. The amplifier performance at 2.5 GHz is shown in Fig. 4. The 3-dB bandwidth is dc to 2.5 GHz with a 50-Ω load, with 7.4 dB saturated gain at 2.5 GHz.

In summary, we have demonstrated the first monolithic integration of p-n-p and n-p-n HBT's using selective MBE to construct a complementary HBT push–pull amplifier. The amplifier shows high dc-functional yield across the wafer, with dc to 2.5 GHz bandwidth. The availability of a high-yield complementary HBT process will allow new applications of HBT technology in the future.

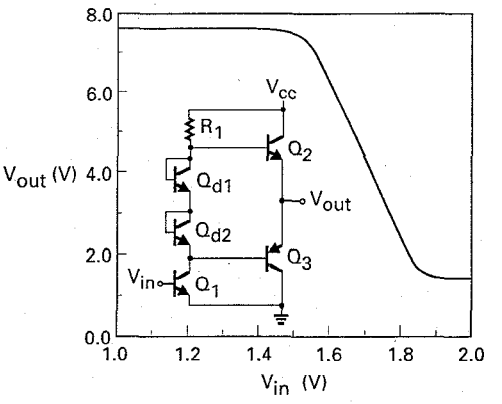

Fig. 3. Push–pull amplifier characteristic curve with $V_{cc} = 9$ V. Insert: Complementary HBT push–pull amplifier schematic.

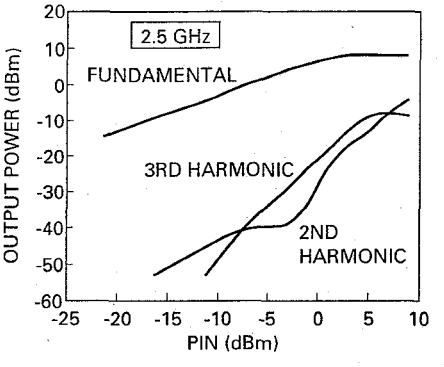

Fig. 4. Complementary HBT push–pull amplifier performance at 2.5 GHz. Saturated output power is 7.4 dBm.

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